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Terms	Documents
(((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)and (malfunction or error)and (synchronizing)and ("signal generator")and (malfunction or error)and (display)	6

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Refine Search: (((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)and (malfunction or error)and Clear

Search History

Today's Date: 10/11/2001

DB Name	Query	Hit Count	Set Name
USPT	(((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)and (malfunction or error)and (synchronizing)and ("signal generator")and (malfunction or error)and (display)	6	L8
USPT	(((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)and (malfunction or error)and (synchronizing)and ("signal generator")and (malfunction or error)	6	L7
USPT	(((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)and (malfunction or error)and (synchronizing)and ("signal generator")	6	L6
USPT	(((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)and (malfunction or error)and (synchronizing)	38	L5
USPT	(((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)and (malfunction or error)	174	L4
USPT	(((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)	402	L3
USPT	(((345/$3).ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)	981	L2
USPT	((345/$3).ccls.) and (lcd)	4136	L1

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Search Results - Record(s) 1 through 6 of 6 returned.

☑ 1. Document ID: US 6198468 B1

L8: Entry 1 of 6 File: USPT Mar 6, 2001

US-PAT-NO: 6198468
DOCUMENT-IDENTIFIER: US 6198468 B1
TITLE: Apparatus for performing various on-screen display functions and methods for each function

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 5874937 A

L8: Entry 2 of 6 File: USPT Feb 23, 1999

US-PAT-NO: 5874937
DOCUMENT-IDENTIFIER: US 5874937 A
TITLE: Method and apparatus for scaling up and down a video image

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 5859392 A

L8: Entry 3 of 6 File: USPT Jan 12, 1999

US-PAT-NO: 5859392
DOCUMENT-IDENTIFIER: US 5859392 A
TITLE: Method and apparatus for reducing noise in an electrostatic digitizing tablet

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 4. Document ID: US 5642134 A

L8: Entry 4 of 6 File: USPT Jun 24, 1997

US-PAT-NO: 5642134
DOCUMENT-IDENTIFIER: US 5642134 A
TITLE: Integrated tablet device having position detecting function and image display function

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 5. Document ID: US 5585864 A

L8: Entry 5 of 6 File: USPT Dec 17, 1996

US-PAT-NO: 5585864
DOCUMENT-IDENTIFIER: US 5585864 A
TITLE: Apparatus for effecting high speed transfer of video data into a video memory using direct memory access

Full | Title | Citation | Front | Review | Classification | Date | Reference | KWIC | Draw Desc | Image

☐ 6. Document ID: US 4532502 A

L8: Entry 6 of 6 File: USPT Jul 30, 1985

US-PAT-NO: 4532502
DOCUMENT-IDENTIFIER: US 4532502 A
TITLE: Apparatus for selectively transferring data between registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | KWIC | Draw Desc | Image

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Terms	Documents
(((345/$3)!.ccls.)) and (lcd)and (pll or phased lock loop or mulfunction)and (converter)and (malfunction or error)and (synchronizing)and ("signal generator")and (malfunction or error)and (display)	6

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L8: Entry 1 of 6 File: USPT Mar 6, 2001

DOCUMENT-IDENTIFIER: US 6198468 B1
TITLE: Apparatus for performing various on-screen display functions and methods for each function

ABPL:
An apparatus having various on-screen display (OSD) functions and methods for each function are provided. The apparatus includes an on-screen display device for receiving serial data having a RAM write address, a ROM address, and the on-screen display functions. The apparatus synthesizes a character signal corresponding to serial data with a background color signal or an external composite video signal in response to an internal or external composite synchronous signal and provides the result to a monitor. The apparatus also includes a synchronous signal generating device for generating internal horizontal and vertical synchronous signals upon receiving a main clock signal, synthesizing means for synthesizing an internal equalization pulse with the internal horizontal and vertical synchronous signals, and means for determining the internal composite synchronous signal or the external composite synchronous signal extracted from the composite video signal. A control device is also part of the OSD apparatus. The control device outputs user serial data to the on-screen display device, generates the main clock signal from a system clock, and controls the on-screen display device and the synchronous signal generating device.

BSPR:
The present invention relates to an on-screen display (OSD), and more particularly, to an apparatus for performing various on-screen display functions for displaying a character on a screen in various forms and a method for performing each function.

BSPR:
An OSD apparatus generates and displays a character in similar manner to a typical liquid crystal display (LCD) controller. However, unlike an LCD controller, the OSD apparatus displays the character together with a moving picture signal.

BSPR:
The OSD apparatus separates and detects horizontal and vertical synchronous signals from a composite synchronous picture signal and uses the detected horizontal and vertical signals as picture synchronous signals. An Automatic Frequency Controller (AFC) is then used to display the character synchronized with the picture signal without scattering or distortion. The AFC is part of the Phase Locked Loop (PLL) and can be any one of various types. Typically, a Frequency Synthesized PLL is used for on screen displays. The PLL is used for compensating for the phase and frequency difference of the external composite video signal. However, in the prior art, the state of synchronous signals included in the external composite video signal is erratic when a pseudo composite video signal including, for example, a guard signal, is input to the frequency synthesized PLL. The PLL cannot compensate well for erratic synchronous signals present in the composite video signal. Also, in a conventional OSD apparatus characters are displayed on a background screen or with a video signal.

BSPR:

It is an object of the present invention to provide an apparatus which performs various on-screen display (OSD) functions.

BSPR:
It is another object of the present invention to provide an apparatus which performs a half-tone conversion function in which a character display region is highlighted by darkening a character relative to a background region.

BSPR:
To achieve an object of the invention there is provided an apparatus for performing a plurality of on-screen display functions on a character. The apparatus includes a control means for receiving user data and a system clock signal and generating serial data and a main clock signal and synchronous signal generating means coupled to said control means for receiving the main clock signal and a composite video signal, generating an equalization pulse and internal horizontal and vertical synchronous signals responsive to the main clock signal, generating an internal composite synchronous signal by synthesizing the internal equalization pulse with the internal horizontal and vertical synchronous signals, and generating an external composite synchronous signal corresponding to the composite video signal. The apparatus also includes on-screen display means for receiving the serial data and either the internal or the external composite synchronous signal from the synchronous signal generating means, generating a character signal responsive to either the internal or the external composite synchronous signals, and providing the character signal to a monitor for displaying the character.

BSPR:
To achieve a further object of the invention there is provided an apparatus for performing a plurality of on-screen display functions, the apparatus receiving a composite video signal and user data, the apparatus including interface means for receiving serial data having a ROM address and at least one on-screen display function and converting the serial data into parallel data and a RAM coupled to said interface means for storing the parallel data. The apparatus also includes a ROM coupled to said RAM for storing character data of a character to be displayed and level adjusting means for generating level-adjusted character data by adjusting the DC level of the character data corresponding to the parallel data. Signal synthesizing means coupled to said level adjusting means for generating a synthesized character signal by synthesizing the level-adjusted character data with either the externally input composite video signal or an internally generated background color signal and providing the synthesized character signal to a monitor for displaying the character.

DRPR:
FIG. 1 is a block diagram of an apparatus performing various on-screen display (OSD) functions according to the present invention;

DEPR:
As shown in FIG. 1, an apparatus performing various OSD functions according to the present invention includes an OSD portion 10, a synchronous signal generating portion 20, and a control portion 30. The OSD portion 10 includes an interface portion 40, a horizontal controller 42, a timing generator 44, a vertical controller 46, an address counter 48, a RAM 50, a ROM 52, a parallel-to-serial data converter 54, a mixer 56, a signal synthesizer 58, a clamp 60, and an output buffer 62. Synchronous signal generating portion 20 includes an internal horizontal synchronous signal generator 80, an internal vertical synchronous signal generator 82, an internal/external composite synchronous signal generator 84, a first external horizontal synchronous signal generator 86, a synchronous signal delaying portion 88, a dot clock signal generator 90, a mask signal generator 92, a second external horizontal synchronous signal generator 94, a phase-locked loop (PLL) 96 and a color generator 98. Mask signal generator 92, second external horizontal synchronous signal generator 94, and Phase-Locked Loop (PLL) 96 constitute video signal compensating portion 100.

DEPR:
Control portion 30 generates a main clock 4 fsc upon receiving a clock signal CK and various control signals for controlling OSD portion 10 and synchronous signal generating portion 20. Control portion 30 determines whether the composite video signal is received externally via input node IN1 and generates a corresponding control signal C2. Control portion 30 provides control signal C2 to external/internal synchronous signal generating portion 84 via interface portion 40. Internal/external composite synchronous signal generating portion 84, in turn, determines whether to output the internal composite synchronous signal or the external composite synchronous signal responsive to control signal C2. That is, internal/external composite synchronous signal generator 84 outputs the internal composite synchronous signal if the external composite video signal is not input and outputs the external composite synchronous signal if the external composite video signal is input.

DEPR:
Interface portion 40 receives serial data SD shown in FIG. 1. Serial data SD can be a RAM write address for writing a ROM address into RAM 50, a ROM address used for storing character data in ROM 52, and control data used for the various OSD functions. Interface portion 40 stores the received RAM write address in, for example, an internal shift register (not shown) responsive to clock signal (shown in FIG. 2A) and outputs the ROM address in parallel by synchronizing the shift register data with the write data clock signal shown in FIG. 2C. Also, interface portion 40 outputs signals required for writing data in RAM 50 and for controlling timing generator 44. Furthermore, interface portion 40 generates blank data from RAM 50 when erasing all data stored in RAM 50.

DEPR:
Horizontal controller 42 generates horizontal signal information, such as the horizontal size and the horizontal start position of the character to be displayed. That is, when the vertical size of a character and vertical start position signal generated from vertical controller 46 are input, a horizontal start position signal is determined according to an internal or external horizontal synchronous signal based on the value of an internal register (not shown). The horizontal size of the character to be displayed is determined by classifying a first line and the remaining lines. Character size data is generated in order to display a maximum of 30 characters in the horizontal direction. In addition, horizontal controller 42 generates an original clock signal according to the selected horizontal character size and outputs the generated clock signal to parallel-to-serial data converter 54.

DEPR:
Timing generator 44 generates timing signals required for reading out data stored in RAM 50. Timing generator 44 receives the horizontal character size and the horizontal character start position signal output from horizontal controller 42 and outputs a boundary timing signal BT and an address timing signal AT to parallel-to-serial data converter 54 and address counter 48, respectively, responsive to the signals generated from interface portion 40.

DEPR:
FIG. 3 shows horizontal and vertical positions HS and VS, respectively, of displayed character 110. Vertical controller 46 outputs the vertical start position signal and the vertical size of the character to be displayed. After an internal or external vertical synchronous signal is input to the internal/external composite synchronous signal generator 84, vertical controller 46 counts a horizonal synchronous signal based on the value of an internal register (not shown) to determine a vertical start position signal. In the same manner, vertical character size is determined by classifying a first line and the remaining lines. Then, vertical controller 46 counts a dot address clock signal generated according to the determined vertical character size to output an enable signal to ROM 52.

DEPR:
Parallel-to-serial data converter 54 receives parallel data output from ROM 52

and serially outputs character and boundary data to mixer 56 or outputs blank data regardless of the data output from ROM 52. Parallel-to-serial data converter 54 additionally receives boundary timing signal BT from timing generator 44 to output boundary blank data. That is, parallel-to-serial data converter 54 outputs boundary blank data after loading the data output from ROM 52 into an internal register (not shown) and after the boundary timing signals are input to an internal register (also not shown). Parallel-to-serial data converter 54 performs the above-mentioned operation responsive to the clock signal generated by horizontal controller 42.

DEPR:
Parallel-to-serial data converter 54 outputs a horizontal display termination signal when the current boundary timing signal is input. Parallel-to-serial data converter 54 also outputs a raster blank signal for disabling the read enable signal when the previous boundary timing signal is input. Parallel-to-serial data converter 54 selects a blank from respective character lines and outputs blank data to mixer 56.

DEPR:
Mixer 56 mixes character data with a video signal. When a composite video signal is externally input, mixer 56 mixes and outputs the character and blank data output from parallel-to-serial data converter 54 with a background color signal output from color generator 98 and a video signal generated from synchronous signal generating portion 20. Color generator 98 receives the internal horizontal synchronous signal from internal/external composite synchronous signal generator 84 and the color information data included in parallel data D output from interface portion 40. Color generator 98 generates a color burst signal corresponding to the internal horizontal synchronous signal responsive to clock signal 4 fsc. Color generator 98 also generates a background color signal responsive to the color information data in parallel data D, a blank color signal, a raster color signal, and other similar color signals.

DEPR:
Synchronous signal generating portion 20 operates as follows. Internal horizontal synchronous signal generator 80 receives clock signal 4 fsc from control portion 30. Internal horizontal synchronous signal generator 80 generates a horizontal synchronous signal having a period corresponding to 910 times that of clock signal 4 fsc, an internal equalizing pulse having a period corresponding to half the period of the horizontal synchronous signal, and an internal horizontal synchronous signal by combining the internal equalizing pulse and the horizontal synchronous signal.

DEPR:
Internal vertical synchronous signal generator 82 receives clock signal 4 fsc and generates an internal vertical synchronous signal having a period corresponding to 2.5 to 3 times that of clock signal 4 fsc.

DEPR:
Internal/external composite synchronous signal generating portion 84 determines whether to output the internal composite synchronous signal or the external composite synchronous signal responsive to control signal C2. That is, internal/external composite synchronous signal generator 84 outputs the internal composite synchronous signal if the external composite video signal is not received by control portion 30 and outputs the external composite synchronous signal if the external composite video signal is received by control portion 30. Internal/external composite synchronous signal generator 84 combines the internal vertical synchronous signal and the internal horizontal synchronous signal to generate an internal composite synchronous signal. Also, internal/external composite synchronous signal generator 84 outputs an external composite synchronous signal by combining the first external horizontal synchronous signal received from first horizontal synchronous signal generator 86 with the internal vertical synchronous signal.

DEPR:
First external horizontal synchronous signal generator 86 extracts a first external horizontal synchronous signal from the composite video signal externally input via input node IN1. First external horizontal synchronous signal generator 86 sends a state signal to internal/external composite synchronous signal generator 84. Internal/external composite synchronous signal generator 84 extracts the external horizontal synchronous signal from the composite video signal responsive to the state signal. If the external horizontal synchronous signal is extracted, internal/external composite synchronous signal generator 84 generates the external composite synchronous signal. That is, internal/external composite synchronous signal generator 84 generates an internal composite synchronous signal by synthesizing the internal vertical synchronous signal output from internal vertical synchronous signal generator 82 and the internal horizontal synchronous signal output from internal horizontal synchronous signal generator 80 responsive to control signal C2. Internal/external composite synchronous signal generator 84 generates an external composite synchronous signal by using the external vertical synchronous signal extracted from the composite video signal received at input node IN1 responsive to control signal C2.

DEPR:
Video signal compensating portion 100 includes mask signal generator 92 for generating a mask signal based on the external horizontal synchronous signal output from the first external horizontal synchronous signal generator 86. Video signal compensating portion 100 also includes PLL 96 and second external synchronous signal generator 94. Second external synchronous signal generator 94 generates a second external horizontal synchronous signal from the mask signal received from mask signal generator 92. PLL 96 compares the phase of the second external horizontal synchronous signal output from second external horizontal synchronous signal generator 94 with the phase of a feedback signal, oscillates the frequency at a rate corresponding to the compared result, multiplies the oscillated frequency by a predetermined value, and outputs the multiplied feedback signal to internal/external composite synchronous signal generator 84 as a third external horizontal synchronous signal.

DEPR:
In an OSD apparatus for adding a character signal to a motion video signal, PLL 96 outputs stable character and display clock signals synchronized with an external video signal. Where the external video signal includes noise components, mask signal generator 92 and second external horizontal synchronous signal generator 94 are additionally coupled to PLL 96, where PLL 96 is of a frequency synthesizer type, in order to remove noise signals which prevent the stabilization of PLL 96. Noise signals can include video track traveling switching noises and copy guard signals.

DEPR:
Internal/external composite synchronous signal generator 84 receives the third external horizontal synchronous signal output from PLL 96. In order to prevent jittering and distortion of the character caused by noise or copy guard signals applied to PLL 96, mask signal generator 92 generates a mask signal based on the external horizontal synchronous signal input thereto. For example, when mask signal generator 92 generates a logic high mask signal noise is removed from the external horizontal synchronous signal when the external horizontal synchronous signal is at a logic low. That is, in order to prevent character distortion induced from excessive phase detection error signals generated by uncompensated video head switching pulses, video signal compensating portion 100 generates a mask signal in a vertical blanking interval to hold the phase direction function of PLL 96 and maintain the central frequency of the voltage control oscillator included therein to a predetermined level within the holding interval thereby providing a stable synchronous signal during character display.

DEPR:
Synchronous signal delaying portion 88 receives an external or internal

composite synchronous signal from internal/external composite synchronous signal generator 84, generates a one-shot horizontal synchronous signal, and outputs one-shot horizontal synchronous signal to dot clock signal generator 90. Generally, the position of a character to be displayed is determined based on the horizontal synchronous signal. The pulse width of the original horizontal synchronous signal may not coincide with the requirements of the system. When this happens, synchronous signal delaying portion 88 generates a one-shot horizontal synchronous signal having a predetermined width meeting the system requirements and which corresponds to the horizontal synchronous signal.

DEPR:
Dot clock signal generator 90 receives the one-shot horizontal synchronous signal and generates a dot clock signal DCLK. The frequency of dot clock signal DCLK, set for displaying a maximum of 30 characters on a screen, is typically 9 MHz. Dot clock signal generator 90 controls the start position and the horizontal size of the character. When the horizontal and vertical position start signals for displaying a character are determined, output data of ROM 52 is displayed on the screen from the start position generated by dot clock signal generator 90. The dot clock signal is related to the size of the character and is used to synchronize outputting ROM 52 data.

DEPR:
ROM 52 shown in FIG. 9 preferably comprises 55.296 KBits (12.times.18.times.256) for a total of 256 characters having a 12.times.18 matrix structure. Using the data output from RAM 50 as the address of ROM 52, eighteen bundles of 256 ROM cells are selected through a word line by a ROM decoder (not shown) and a bit line is selected by an internal column decoder (not shown) to output 12 bits of ROM data on ROM output signal ROM_OUT. The 12 bits of parallel ROM data are output to mixer 56 via parallel-to-serial data converter 54 as character and blank data.

DEPR:
Methods for performing various OSD functions, including a half-tone box drawing, scroll, blink, and other functions using the OSD apparatus shown in FIG. 1 will be described with reference to FIGS. 11 to 13. The half-tone OSD function is used for highlighting a character displayed in a background screen by making the character display region 130 relatively darker than a non-character display region 140 where characters are not displayed. To do so, parallel-to-serial data converter 54 adjusts the DC level of the character data to be displayed according to the control data input from interface portion 40 and outputs a level-adjusted signal to mixer 56. Signal synthesizer 58 synthesizes the DC-level adjusted character data with composite video data input from clamp 60 and outputs the synthesized signal to output node OUT via output buffer 62 to display the character shown in FIG. 11.

DEPR:
The box drawing OSD function will be described with reference to FIG. 12. The box drawing function is used for highlighting a character or sentence displayed in three dimensions by surrounding it with a rectangular border. Parallel-to-serial data converter 54 generates box data based on the character or sentence data according to the control data input from interface portion 40 which determines whether to provide a protruded cubic effect or a recessed cubic effect to the displayed character or sentence. When providing the protruded cubic effect to the displayed character or sentence, the DC level adjuster (not shown) included in parallel-to-serial data converter 54 adjusts the DC level of the data located at lower right side 150 of the box as shown in FIG. 12 and outputs the result to mixer 56. When providing the recessed cubic effect, the DC level adjuster adjusts the DC level of the data located at upper left side 160 of the box as shown in FIG. 12 and outputs the result to mixer 56.

DEPR:
Signal synthesizer 58 synthesizes the box data, character data, and composite video data input from clamp 60 and outputs the synthesized signal to output

node OUT via output buffer 62 to display the picture shown in FIG. 12.

DEPR:
The scroll OSD function will be described with reference to FIG. 13. According to the scroll OSD function, whether the character is on or off is controlled by displaying the character line by line in sequence thereby improving the visual effect of the displayed character. For example, the character `0` is displayed in sequence line by line in the arrow direction as shown in FIG. 13. To display a scrolled character, data stored in ROM 52 is read according to the dot address signal and the dot clock signal generated according to the vertical character start position signal and the vertical character size in vertical controller 46 shown in FIG. 1. Parallel-to-serial data converter 54 serially outputs the data read from ROM 52 according to the dot address signal and the dot clock signal to mixer 56 in response to the scroll control signal.

DEPR:
The scroll control signal is generated from a scroll controller (not shown) included in parallel-to-serial data converter 54. The scroll controller outputs the scroll control signal for controlling scroll time and a scroll on/off function according to the control data input from interface portion 40.

DEPR:
Mixer 56 mixes the internal or external composite synchronous signal, a background color signal, and data output from parallel-to-serial data converter 54 and outputs the result to signal synthesizer 58. The signal synthesizer 58 synthesizes the output from mixer 56 with the composite video signal input via clamp 60 during a scroll time interval and outputs the synthesized signal to output node OUT via output buffer 62 to display the picture shown in FIG. 13.

DEPR:
The blink OSD function is used for highlighting a displayed character by causing it to blink. To blink the displayed character, parallel-to-serial data converter 54 determines whether to perform the blinking function according to the control data input from interface portion 40. When performing the blinking function, the blink controller (not shown) included in parallel-to-serial data converter 54 outputs a blink control signal for controlling blinking time and intensity according to the input control data. Parallel-to-serial data converter 54 alternatively outputs to mixer 56 either blink data or character data input in parallel from ROM 52 responsive to the blink control signal.

DEPR:
Mixer 56 mixes the internal or external composite synchronous signal, a background color signal, and data alternatively output from parallel-to-serial data converter 54 and outputs the result to signal synthesizer 58. Signal synthesizer 58 synthesizes blank data and character data output from mixer 56 with the composite video signal input from clamp 60, and outputs the synthesized signal to output node OUT via-output buffer 62 to display a picture on a monitor (not shown).

DEPR:
As described above, 256 various characters can be displayed with a maximum of 300 displayed characters in a single screen using the OSD apparatus of the present invention. Signal compensating portion 100 compensates for recorder/reproducer misoperation by synchronizing the video signal and the character to be displayed on a screen without jittering and/or distortion. In addition, in order to satisfy various user demands, a character coloring, half-tone, scroll, box drawing, character start point control, character size control, blank region coloring, and blinking functions are provided by the OSD apparatus of the present invention. The OSD apparatus also outputs a composite video signal which is compatible with other video systems. Finally, the OSD apparatus of the present invention improves the driving performance of the output node by including an output buffer and reduces cost and improves

reliability by being realized with a single chip.

CLPR:
1. An apparatus for performing a plurality of on-screen display functions on a character, the apparatus comprising:

CLPR:
2. An apparatus for performing a plurality of on-screen display functions on a character, the apparatus comprising:

CLPR:
7. The apparatus of claim 5 wherein said composite synchronous signal generator includes an internal/external composite synchronous signal generator for generating the internal composite synchronous signal by synthesizing the internal horizontal synchronous signal with an internal vertical synchronous signal, the internal vertical synchronous signal having a predetermined period corresponding to a period of the horizontal synchronous signal, generating the external composite synchronous signal responsive to the composite video signal, providing the internal composite synchronous signal to said mixer, and providing the internal or external composite synchronous signal to said vertical controller.

CLPR:
8. The apparatus of claim 6 wherein said composite synchronous signal generator includes an internal/external composite synchronous signal generator for generating the internal composite synchronous signal by synthesizing the internal horizontal synchronous signal with an internal vertical synchronous signal, generating the external composite synchronous signal responsive to either the first or third external horizontal synchronous signal, providing the internal composite synchronous signal to said mixer, and providing the external composite synchronous signal to said vertical controller.

CLPR:
11. The apparatus of claim 2 wherein said on-screen display means further includes level adjusting means for generating a level-adjusted composite video signal by adjusting a voltage level of the composite video signal and providing the level-adjusted composite video signal to said signal synthesizer.

CLPR:
13. The apparatus of claim 5 wherein said synchronous signal generating means further comprises a color generator coupled to said composite synchronous signal generator and said interface portion for generating a color burst signal corresponding to the internal horizontal synchronous signal and a background color signal corresponding to color information data contained in the parallel data, said color generator providing the color burst signal and the background color signal to said mixer responsive to the main clock.

CLPR:
14. An apparatus for performing a plurality of on-screen display functions, the apparatus receiving a composite video signal and user data, the apparatus comprising:

CLPR:
15. The apparatus of claim 14 wherein the serial data includes a half-tone on-screen display function which displays a region in which the character is shown relatively darker than a region in which the character is not shown.

CLPR:
16. The apparatus of claim 14 wherein the serial data includes a box drawing on-screen display function which displays the character or a sentence bounded by a box and including a data generator coupled to said interface means for generating box data corresponding to the parallel data.

CLPR:

17. The apparatus of claim 14 wherein the serial data includes a scroll on-screen display function which displays the character in line-by-line sequence and including:

CLPR:
18. The apparatus of claim 14 wherein the serial data includes a blink on-screen display function for blinking the displayed character and including:

CLPR:
19. A method for performing a plurality of on-screen display functions in an apparatus, the apparatus including a ROM and a RAM, the method comprising:

CLPR:
20. The method of claim 19 wherein the user data includes a half-tone on-screen display function which displays a region in which the character is shown relatively darker than a region in which the character is not shown, the method including:

CLPR:
21. The method of claim 19 wherein the user data includes a box drawing on-screen display function which displays the character or a sentence bounded by a box, the method including generating box data corresponding to the user data before generating a displayed character signal and wherein generating a displayed character signal includes synthesizing the box data with the character data and either the composite video signal or the background color signal.

CLPR:
23. The method of claim 19 wherein the user data includes a scroll on-screen display function which displays the character in line-by-line sequence, the method including:

CLPR:
24. The method of claim 19 wherein the user data includes a blink on-screen display function for blinking the displayed character, the method including:

CLPV:
on-screen display means for receiving the serial data and either the internal or the external composite synchronous signal from the synchronous signal generating means, generating a character signal responsive to either the internal or the external composite synchronous signals, and providing the character signal to a monitor for displaying the character.

CLPV:
on-screen display means for receiving the serial data and either the internal or the external composite synchronous signal from the synchronous signal generating means, generating a character signal responsive to either the internal or the external composite synchronous signals, and providing the character signal to a monitor for displaying the character;

CLPV:
wherein said on-screen display means includes:

CLPV:
a first external horizontal synchronous signal generator for extracting the external horizontal synchronous signal from the composite video signal; and

CLPV:
a composite synchronous signal generator coupled to said first external horizontal synchronous signal generator for generating the internal composite synchronous signal and the internal equalization pulse responsive to the main clock signal and generating the external composite synchronous signal responsive to the external horizontal synchronous signal.

CLPV:
a mask signal generator coupled to said first external horizontal synchronous signal generator for generating a mask signal corresponding to the external horizontal synchronous signal;

CLPV:
a second external horizontal synchronous signal generator coupled to said mask signal generator for generating a second external horizontal synchronous signal corresponding to the mask signal; and

CLPV:
a phase locked loop coupled to said second external horizontal synchronous signal generator for determining a frequency difference between the second external horizontal synchronous signal and a feedback signal, generating a third horizontal synchronous signal having a frequency substantially equal to the frequency difference multiplied by a predetermined value, and providing the third external horizontal synchronous signal to said composite synchronous signal generator.

CLPV:
a dot clock signal generator for generating a dot clock signal of the character to be displayed upon receiving the one-shot horizontal synchronous signal.

CLPV:
a dot clock signal generator for generating a dot clock signal of the character to be displayed upon receiving the one-shot horizontal synchronous signal.

CLPV:
interface means for receiving serial data having a ROM address and at least one on-screen display function and converting the serial data into parallel data;

CLPV:
a parallel-to-serial data converter for converting character data received in parallel from said ROM to serial character data responsive to the scroll control signal;

CLPV:
a mixer coupled to said parallel-to-serial data converter for generating a mixer signal by mixing the background color signal and the serial character data; and

CLPV:
a parallel-to-serial data converter for converting character data received in parallel from said ROM to serial character data and alternatively providing to said signal synthesizer character blink data or the serial character data responsive to the blink control signal.

CLPV:
receiving user data having a ROM address at which character data is stored and an on-screen display function for displaying a character on a monitor;

CLPV:
using the displayed character signal to display the character on the monitor.

CLPV:
wherein using the displayed character signal includes using the scroll time to display the character on the monitor.

CLPW:
a parallel-to-serial data converter coupled to said horizontal converter for converting parallel character data received from said ROM to serial character data and providing either the serial character data or blank data to a

parallel-to-serial converter output node responsive to the horizontal clock signal or the boundary timing signal;

CLPW:
a mixer for generating a mixer signal by mixing either the internal or the external composite synchronous signal and either the serial character data or the blank data output from said parallel-to-serial data converter; and

CLPW:
a signal synthesizer for generating a synthesized signal by synthesizing the mixer signal with the composite video signal and providing the synthesized signal to the display.

CCOR:
345/467